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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,492	03/01/2004	Nobuaki Hashimoto	118876	9029

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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/788,492	HASHIMOTO, NOBUAKI	
	Examiner	Art Unit	
	Matthew C. Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-10,17,18 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-10* is/are allowed.

6)☒ Claim(s) *1,2,17,18 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 5, 2008 has been entered.

Claim Objections

Claims 1, 20, and 23 are objected to because of the following informalities:

Regarding claims 1 and 20, the limitation "the connecting layer and the insulating section is formed integrally" should be changed to "the connecting layer and the insulating film are formed integrally".

Further regarding claim 20, the limitation "interconnect patter" in line 2 of the claim should be changed to "interconnect pattern". Appropriate correction is required.

Regarding claim 23, the limitation "The method or manufacturing" should be changed to "The method of manufacturing".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 23 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation "the first portion having a lower surface than the top surface" renders the claim indefinite. It is unclear what structure the limitation intends to describe. Does Applicant intend to claim the structure shown in Figure 4 of the instant application, where a portion of the insulating section 40 is in contact with an upper surface of the chip component? Or is some other interpretation of the claim desired?

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 23 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation "the second part has a first portion disposed on the passivation film and a second portion disposed adjacent to the chip component, the first portion having a lower surface than the top surface" (in combination with the newly added limitations of claim 5) is not sufficiently supported by the originally filed application. The new limitations of claim 5 read only on the embodiment shown in Figure 7. However, the insulating section in Figure 7 does not appear to have a "first portion having a lower surface than the top surface". Therefore, this limitation constitutes new matter. Note that the upper portion of insulating section 60 (Fig. 7) could still be

considered "on" the passivation layer 12 since it is in contact with a side surface. However, if Applicant intended "on" to mean "above", or "on top of", then the limitation "disposed on the passivation film" would also be new matter.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 17, 18, 20, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeung et al. (US Pat. 6,747,348, hereinafter Jeung) in view of Ling et al. (US Pat. 6,445,069, hereinafter Ling).

Regarding claims 1 and 20, Figure 4L of Jeung discloses a substrate 30 on which an interconnect pattern (pads 23) is formed; a chip component 22 that has a base material, the chip component having a first surface on which a pad 21 is formed and a second surface opposite to the first surface, the chip component being mounted in such a manner that the second surface faces the substrate; a passivation film (section of layer 42 between pads 21) that is formed on the first surface of the chip component, the passivation film formed to avoid at least a part of the pad; an insulating section (portions of layer 42 on the side of the chip) is formed adjacent to the chip component, the insulating section being formed to come to an end at a position a distance away from the pad, the insulating section having a convex surface that draws a curve on a view

from which a cross section perpendicular to the first surface of the chip component is taken, the convex surface ascending from the first surface to have a top surface and descending from the top surface in an outward direction; a connecting layer 34 that is disposed between the second surface of the chip component and the substrate, the connecting layer being formed in such a manner that the connecting layer and the insulating section are formed integrally; and an interconnect 49 that is formed to extend from above the pad to above the interconnect pattern, the interconnect having a first section disposed on the passivation film and a second section disposed over the insulating section, the interconnect covering all lateral surfaces of the pad. Note that the insulating section 42 and the connecting layer 34 can be considered "integrally formed" since the are in contact with each other, forming a "whole". Further, both layers are formed of dielectric material. Together they can be considered a dielectric structure, with each part being "integral" to the dielectric structure as a whole.

Jeung does not disclose a metal layer formed of a plurality of layers including a diffusion prevention layer in contact with the pad and an uppermost layer being less oxidizable than the pad, the diffusion preventing layer preventing any diffusion of material formed thereabove into the base material of the chip component. Ling discloses a chip component 10 of a base material having a first surface on which a pad 26 is formed and metal layer 32/34/36 formed of a plurality of layers including a diffusion prevention layer 32/34 in contact with the pad and an uppermost layer 36 being less oxidizable than the pad, the diffusion prevention layer preventing any diffusion of material formed thereabove into the base material of the chip component. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Jeung by forming a metal layer such as that taught by Ling. The

motivation for doing so is to allow the use of copper interconnect metallization while facilitating the electrical coupling of connection pads to supporting substrates or other packaging while using known metal deposition processes in a simple and inexpensive manner that is compatible with gold bond wires, solder bumps, and other common circuit connection methods and that allows tight spacings between adjacent connections pads without compromising the reliability of the integrated circuit.

Regarding claim 17, it would have been obvious to mount the device of Jeung on a printed circuit board, since such a packaging configuration is extremely well known in the art and allows for integration of several different devices on a single board.

Regarding claim 18, the device of Jeung is considered an electronic instrument.

Regarding claim 25, Figure 4L of Jeung discloses the insulating section (portions of layer 42 on side of chip) has an edge disposed between the pad 21 and a part of the periphery of the chip component on which the insulating section is disposed, the edge being closest of the insulating section to the pad.

Regarding claims 26 and 27, it would have been further obvious to form the insulating section and the connecting layer from the same material to simplify the production process. Further, it has been held that simple substitution of one known element for another to yield predictable results is merely an obvious modification. *KSR International Co. v Teleflex Inc.,* 82 USPQ2d 1385 (2007).

Claims 1, 17-20, 21, 22, and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeung et al. (US Pat. 6,750,547, hereinafter Jeung'547) in view of Ling and Jeung.

Regarding claims 1 and 20, Figure 1G of Jeung'547 discloses a substrate 120 on which an interconnect pattern is formed; a chip component 130 that has a base material, the chip component having a first surface on which a pad 133 is formed and a second surface opposite to the first surface, the chip component being mounted in such a manner that the second surface faces the substrate; a passivation film 134 that is formed on the first surface of the chip component, the passivation film formed to avoid at least a part of the pad; an insulating section 135 that is formed adjacent to the chip component, the insulating section being formed to come to an end at a position a distance away from the metal layer; a connecting layer 125 that is disposed between the second surface of the chip component and the substrate, the connecting layer being formed in such a manner that the connecting layer and the insulating section are formed integrally; and an interconnect 49 that is formed to extend from above the pad to above the interconnect pattern, the interconnect having a first section disposed on the passivation film and a second section disposed over the insulating section, the interconnect covering all lateral surfaces of the pad. Note that the insulating section 135 and the connecting layer 125 can be considered "integrally formed" since the are in contact with each other, forming a "whole". Further, both layers are formed of dielectric material. Together they can be considered a dielectric structure, with each part being "integral" to the dielectric structure as a whole.

Jeung'547 does not disclose a metal layer formed of a plurality of layers including a diffusion prevention layer in contact with the pad and an uppermost layer being less oxidizable

than the pad, the diffusion preventing layer preventing any diffusion of material formed thereabove into the base material of the chip component. Ling discloses a chip component 10 of a base material having a first surface on which a pad 26 is formed and metal layer 32/34/36 formed of a plurality of layers including a diffusion prevention layer 32/34 in contact with the pad and an uppermost layer 36 being less oxidizable than the pad, the diffusion prevention layer preventing any diffusion of material formed thereabove into the base material of the chip component. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Jeung by forming a metal layer such as that taught by Ling. The motivation for doing so is to allow the use of copper interconnect metallization while facilitating the electrical coupling of connection pads to supporting substrates or other packaging while using known metal deposition processes in a simple and inexpensive manner that is compatible with gold bond wires, solder bumps, and other common circuit connection methods and that allows tight spacings between adjacent connections pads without compromising the reliability of the integrated circuit.

Jeung'547 does not explicitly disclose the insulating section having a convex surface. However, Jeung'547 discloses the insulating section 135 can be formed using a viscous type of dielectric material (col. 4, lines 18-25). When using this type of dielectric material, the dielectric layer 135 would not have the sharp corners shown in Figure 1G, unless some other etching/shaping process was performed (which Jeung'547 does not disclose). Clearly, Figure 1G is just a simplified diagram and does not represent the real world actuality. In reality, the corners would be more rounded and therefore have the convex shape claimed. Regardless, Figure 4L of Jeung specifically discloses an insulating section 42 having the claimed convex shape. In view

of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Jeung'547 by using the convex shape taught by Jeung for the insulating section for at least the purpose of simplifying the production process (since no additional etching/shaping process would be required, as is required to obtain the sharp corners shown in Figure 1G of Jeung'547). Furthermore, the mere change in shape recited in the claims is considered obvious to one of ordinary skill in the art as it requires only a minor modification of the shape in Jeung'547 that does not result in any difference in operation or effect. *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Regarding claim 17, Figure 2E of Jeung'547 discloses a printed circuit board 180 on which the electronic device of claim 1 is mounted.

Regarding claim 18, the device of Jeung'547 is considered an electronic instrument.

Regarding claims 21 and 24, Figure 1G of Jeung'547 discloses the insulating section 135 has a first portion disposed on the passivation film 134 and a second portion disposed adjacent to the chip component.

Regarding claim 22, Figure 1G of Jeung'547 discloses a part of the passivation film on which the first section of the interconnect is disposed being between the pad and the insulating section.

Regarding claim 25, Figure 1G of Jeung'547 further discloses the insulating section having an edge disposed between the pad and a part of the periphery of the chip component on which the insulating section is disposed, the edge being closest of the insulating section to the pad.

Regarding claims 26 and 27, it would have been further obvious to form the insulating section and the connecting layer from the same material to simplify the production process. Further, it has been held that simple substitution of one known element for another to yield predictable results is merely an obvious modification. *KSR International Co. v Teleflex Inc.,* 82 USPQ2d 1385 (2007).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeung'547 in view of Ling and Jeung as applied to claim 1 above, and further in view of Tanabe (JP 01-164044).

Regarding claim 2, Jeung'547 does not specifically disclose the insulating section being formed of resin. Tanabe discloses forming an insulating section in a configuration similar to that of Jeung'547 in that it is formed on the substrate 1 and along the side of the chip 4 to surround the chip. Tanabe discloses the insulating section being formed of resin. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of to employ a resin as taught by Tanabe for the insulating section of Jeung'547. It has been held that the use of conventional materials to perform their known functions in a conventional process is obvious. *In Re Raner* 134 USPQ 343 (CCPA 1962). Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In Re Leshin*, 15 USPQ 416.

Allowable Subject Matter

Claims 5-10 are allowed.

The following is an examiner's statement of reasons for allowance: the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including applying a compressive force between the substrate and the chip component so that the insulating adhesive has a first part and a second part, the second part being disposed adjacent to the chip component, the second part having a convex surface that draws a curve on a view from which a cross section perpendicular to the first surface of the chip component is taken, the convex surface ascending from the first surface to have a top surface and descending from the top surface in an outward direction.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments filed March 5, 2008 have been fully considered but they are not persuasive.

Applicant argues that the cited references do not teach a connecting layer as claimed. However, as explained in the above rejection, Jeung discloses a connecting layer 34 and Jeung'547 also discloses a connecting layer 125. With regard to Jeung, the insulating section 42 and the connecting layer 34 can be considered "integrally formed" since the are in contact with each other, forming a "whole". Further, both layers are formed of dielectric material. Together they can be considered a dielectric structure, with each part being "integral" to the dielectric

structure as a whole. With regard to Jeung'547, the insulating section 135 and the connecting layer 125 can be considered integrally formed for the same reasons give above with respect to Jeung.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew C. Landau/
Primary Examiner, Art Unit 2815